REMARKS

Claims 1-20 are pending in the present application. Claims 11-20 have been withdrawn in response to an earlier restriction requirement. Claims 1, 2, 4, and 8 have been amended to correct typographic errors and/or to further clarify the subject matter recited therein. No new matter is added by the amendments, which find support throughout the specification and figures. In particular, the amendments are supported at page 16, lines 7-17; page 22, line 18 to page 23, line 5; and transistor WT1 of figure 1 of the present application. In view of the amendments and the following remarks, favorable reconsideration of this application is respectfully requested.

Applicant notes with appreciation that the Examiner acknowledges that claims 3-10 are directed to patentable subject matter.

The Office Action objects to various informalities in claim 8. Claim 8 has been amended as suggested by the Examiner and therefore it is respectfully submitted that claim 8 is in condition for allowance.

Claims 1 and 2 stand rejected under 35 U.S.C. §102 (e) as anticipated by United States Patent No. 6,532,163 to Okazawa (hereinafter Okazawa). Applicant respectfully traverse.

Claim 1 as amended relates to a Magnetic random access memory (MRAM) that includes, *inter alia*, a ***selecting transistor*** having a first electrode connected to the first wiring and ***a second electrode connected to a power voltage potential supply node*** for controlling the write current.

The Office Action asserts that SB11, SB1n discloses the first wiring and that BT11, BT1n discloses the selecting transistor in figure 4 of Okazawa . However, there is no disclosure or suggestion of a second electrode of a selecting transistor being connected to a power voltage potential supply node, as recited in amended claim 1. In Okazawa, the electrode of transistors

BT11 and BT1n not connected to SB11 and SB1n, respectively, is apparently connected to wiring designated by MB1 and MBn, respectively. As discussed in Okazawa, MB1 and MBn relate to "main bit lines," (Okazawa; col. 8., line 9), which are plainly not power supply voltage nodes. In contrast, in amended claim 1, a first electrode of a selecting transistor is connected to the first wiring and a second electrode of the selecting transistor is connected to ***a power voltage potential supply node***. Since Okawaza fails to disclose or suggest the feature of a second electrode of the selecting transistor being connected to a power supply, Okazawa does not anticipate claim 1.

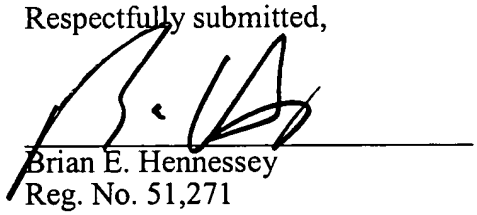
Claim 2 depends from claim 1 and is therefore allowable for at least the same reasons as claim 1 is allowable.

CONCLUSION

In view of the remarks set forth above, this application is believed to be in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290..

Respectfully submitted,



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